19-4103; Rev 0; 5/08

Component Analog TV Sync Separators

General Description

The MAX9566–MAX9569 family of video sync separators extract sync timing information from standard-definition (SDTV), extended-definition (EDTV), and high-definition (HDTV) component video signals. These devices are designed for reliable operation in the presence of copy protection schemes such as MACROVISION®.

The MAX9566–MAX9569 are stand-alone devices and require no external components for timing or biasing. High-impedance video inputs prevent loading of the input signal and eliminate the need for buffering.

The MAX9566/MAX9567/MAX9569 are available in an 8-pin TDFN package, and the MAX9568 is available in a 16-pin QSOP package. All devices are specified over the -40°C to +85°C temperature range.

Applications

Video Digitizers	LCD Displays
Instrumentation	Frame Grabbers
PDP Television	Video Recorders

MACROVISION is a registered trademark of Macrovision Corp.

Features

- ♦ **Stand-Alone Operation—No Timing Element Required**
- ♦ **Covers All Major Standards: SDTV, EDTV, and HDTV**
- ♦ **Identification of Input Standard (MAX9568/MAX9569)**
- ♦ **Loss of Video Signal Detection (MAX9567/MAX9568/MAX9569)**
- ♦ **Coast and Clamp Pulse Outputs**
- ♦ **High-Impedance Bridging Video Input**
- ♦ **No Distortion to Video Signal**
- ♦ **Low Quiescent Current (< 10mA)**
- ♦ **2.7V to 5.5V Single Supply**

Ordering Information

PART	PIN-PACKAGE	TOP MARK
MAX9566ETA+T*	8 TDFN-EP**	ASX
MAX9567ETA+T*	8 TDFN-EP**	ASY

Ordering Information continued at end of data sheet.

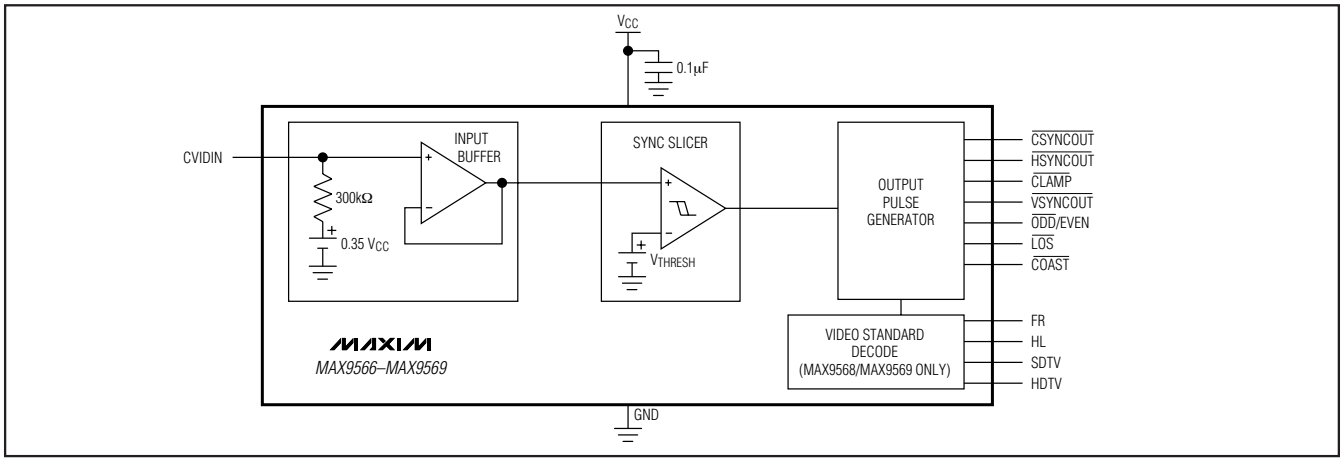
Note: *All devices are specified over the -40°C to +85°C operating temperature range.*

+Denotes a lead-free package.
T = Tape and reel.
**Future product—contact factory for availability.*
***EP = Exposed pad.*

Selector Guide

PART	CLAMP PULSE	$\overline{\text{ODD}}$/EVEN FIELD DETECT	NO SYNC SIGNAL DETECT	COAST	STANDARD IDENTIFICATION	HSYNC, VSYNC AND CSYNC OUTPUTS
MAX9566	Yes	Yes	No	No	No	Yes
MAX9567	Yes	No	Yes	No	No	Yes
MAX9568	Yes	Yes	Yes	Yes	Yes	Yes
MAX9569	No	No	Yes	No	Yes	Yes

Functional Diagram



Component Analog TV Sync Separators

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to GND) .....-0.3V to +6V
All Other Pins to GND .....-0.3V to (V_{CC} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
8-Pin TDFN (derate 18.2mW/°C above +70°C) 1482mW
16-Pin QSOP (derate 8.3mW/°C above +70°C) 667mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{GND} = 0V, T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS							
Supply Voltage Range	V_{CC}	Inferred from horizontal pulse delay		2.7		5.5	V
Supply Current	I_{CC}	With 720p video standard input			8.5	13.5	mA
Input-Voltage Range (Note 2)	V_{IN}	Peak-to-peak video amplitude		0.5		2.0	V
		Absolute range		0.2		V_{CC} - 0.2	
Slice Level	V_{SLICE_BI}	Bilevel syncs		60	95	130	mV
	V_{SLICE_TRI}	Trilevel syncs		110	145	180	
Input Resistance	R_{IN}				300		kΩ
Input DC Bias Voltage	V_B			0.31 x V_{CC}		0.39 x V_{CC}	V
DIGITAL LOGIC OUTPUTS							
Output-Voltage High	V_{OH}	I_{OUT} = 1.6mA	V_{CC} = 5V	4.6			V
			V_{CC} = 2.7V	2.1			
Output-Voltage Low	V_{OL}	I_{OUT} = 1.6mA	V_{CC} = 5V			0.4	V
			V_{CC} = 2.7V			0.5	
AC ELECTRICAL CHARACTERISTICS							
Input Capacitance	C_{IP}				8		pF
Jitter	t_{JITTER}	$\overline{HSYNCOUT}$ output jitter with respect to sync input for 720p video signal			500		ps
Output Logic Rise and Fall Times	t_R, t_F	C_L = 15pF			5		ns

TIMING CHARACTERISTICS

(V_{CC} = +5V, V_{GND} = 0V, T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
525i (Figures 1a and 2a)						
Horizontal Pulse Delay	t_{HP}			20		ns
Horizontal Pulse Width	t_{HPW}			4.8		µs
Clamp Pulse Delay	t_{CP}			570		ns
Clamp Pulse Width	t_{CPW}			3.7		µs
Composite Sync Output Leading Edge Delay	t_{LE}			15		ns
Composite Sync Output Trailing Edge Delay	t_{TE}			15		ns
Vertical Pulse Delay	t_{VP}			20		ns
Vertical Pulse Width	t_{VPW}	Odd/even field		190/122		ns
625i (Figures 1b and 2a)						
Horizontal Pulse Delay	t_{HP}			20		ns
Horizontal Pulse Width	t_{HPW}			4.8		µs
Clamp Pulse Delay	t_{CP}			570		ns
Clamp Pulse Width	t_{CPW}			3.7		µs
Composite Sync Output Leading Edge Delay	t_{LE}			15		ns
Composite Sync Output Trailing Edge Delay	t_{TE}			15		ns
Vertical Pulse Delay	t_{VP}			20		ns
Vertical Pulse Width	t_{VPW}			160/192		ns
525p/480p (Figures 1c and 2a)						
Horizontal Pulse Delay	t_{HP}			20		ns
Horizontal Pulse Width	t_{HPW}			2.4		µs
Clamp Pulse Delay	t_{CP}			290		ns
Clamp Pulse Width	t_{CPW}			1.6		µs
Composite Sync Output Leading Edge Delay	t_{LE}			15		ns
Composite Sync Output Trailing Edge Delay	t_{TE}			15		ns
Vertical Pulse Delay	t_{VP}			20		ns
Vertical Pulse Width	t_{VPW}			190		ns
625p/576p (Figures 1d and 2a)						
Horizontal Pulse Delay	t_{HP}			20		ns
Horizontal Pulse Width	t_{HPW}			2.4		µs
Clamp Pulse Delay	t_{CP}			290		ns

TIMING CHARACTERISTICS (continued)

(V_{CC} = +5V, V_{GND} = 0V, T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clamp Pulse Width	t_{CPW}			1.6		µs
Composite Sync Output Leading Edge Delay	t_{LE}			15		ns
Composite Sync Output Trailing Edge Delay	t_{TE}			15		ns
Vertical Pulse Delay	t_{VP}			20		ns
Vertical Pulse Width	t_{VPW}			192		ns
720p (Figures 1e and 2b)						
Horizontal Pulse Delay	t_{HP}			20		ns
Horizontal Pulse Width	t_{HPW}			540		µs
Clamp Pulse Delay	t_{CP}			1.0		ns
Clamp Pulse Width	t_{CPW}			1.25		µs
Composite Sync Output Leading Edge Delay	t_{LE}			15		ns
Composite Sync Output Trailing Edge Delay	t_{TE}			15		ns
Vertical Pulse Delay	t_{VP}			25		ns
Vertical Pulse Width	t_{VPW}			110		ns
1080i (Figures 1f and 2b)						
Horizontal Pulse Delay	t_{HP}			20		ns
Horizontal Pulse Width	t_{HPW}			585		µs
Clamp Pulse Delay	t_{CP}			1.1		ns
Clamp Pulse Width	t_{CPW}			1.2		µs
Composite Sync Output Leading Edge Delay	t_{LE}			15		ns
Composite Sync Output Trailing Edge Delay	t_{TE}			15		ns
Vertical Pulse Delay	t_{VP}			25		ns
Vertical Pulse Width	t_{VPW}			160/192		ns

Note 1: All devices are production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 2: Input voltage range is guaranteed by the horizontal pulse delay.

Timing Diagrams

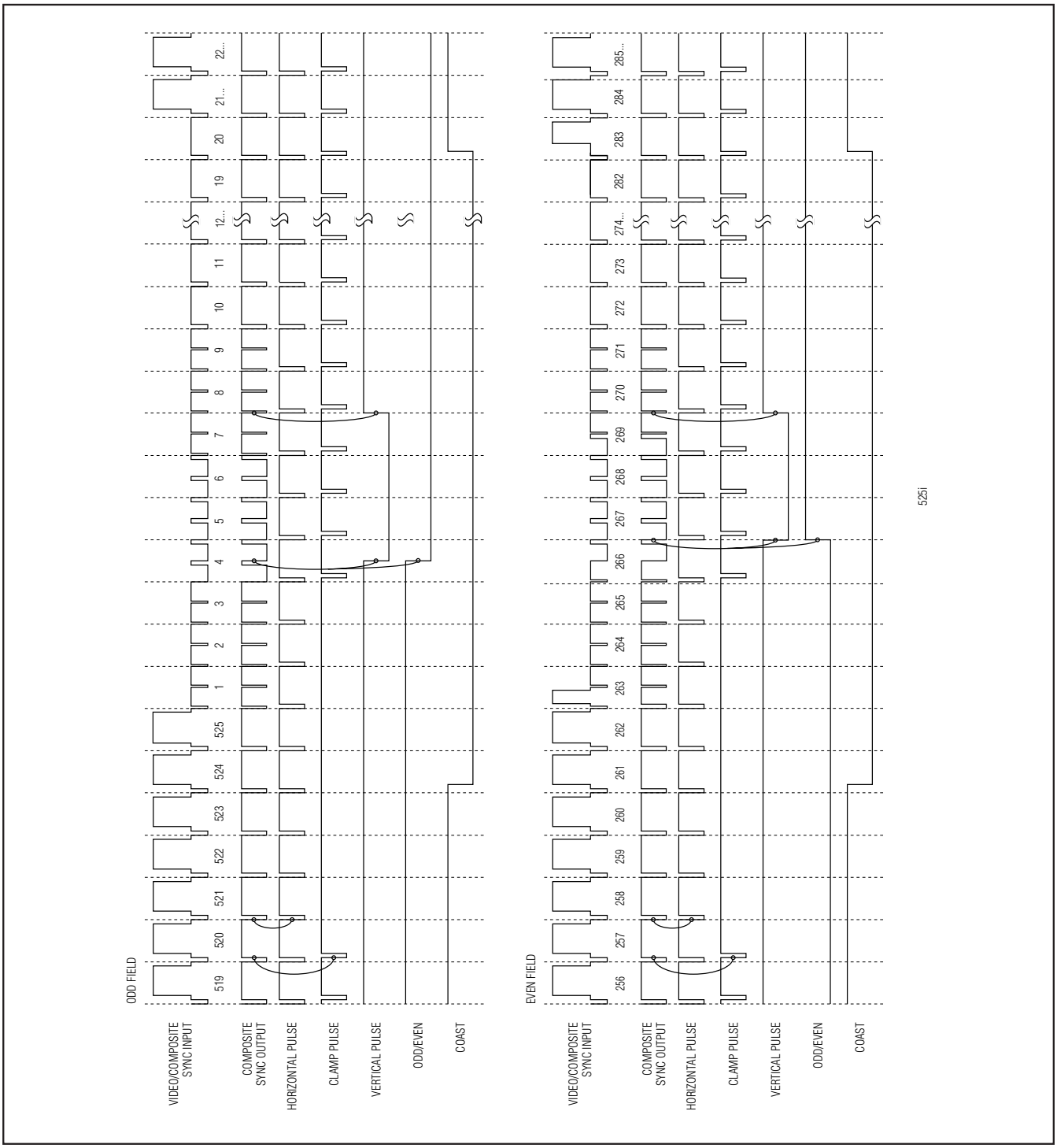


Figure1a. Standard Interlaced 525i (NTSC) Component Video

Component Analog TV Sync Separators

Timing Diagrams (continued)

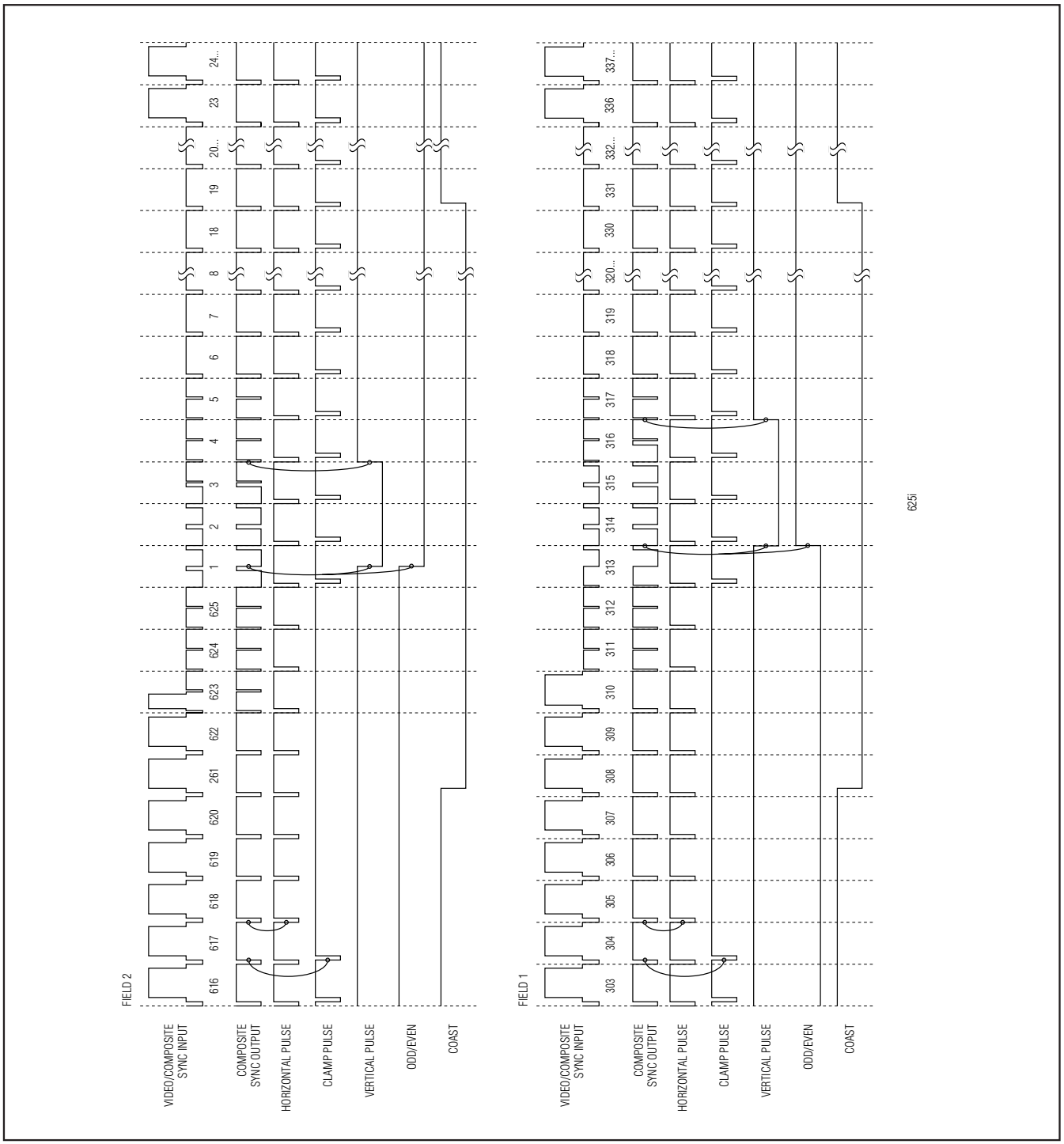


Figure 1b. Standard Interlaced 625i (PAL) Component Video

Timing Diagrams (continued)

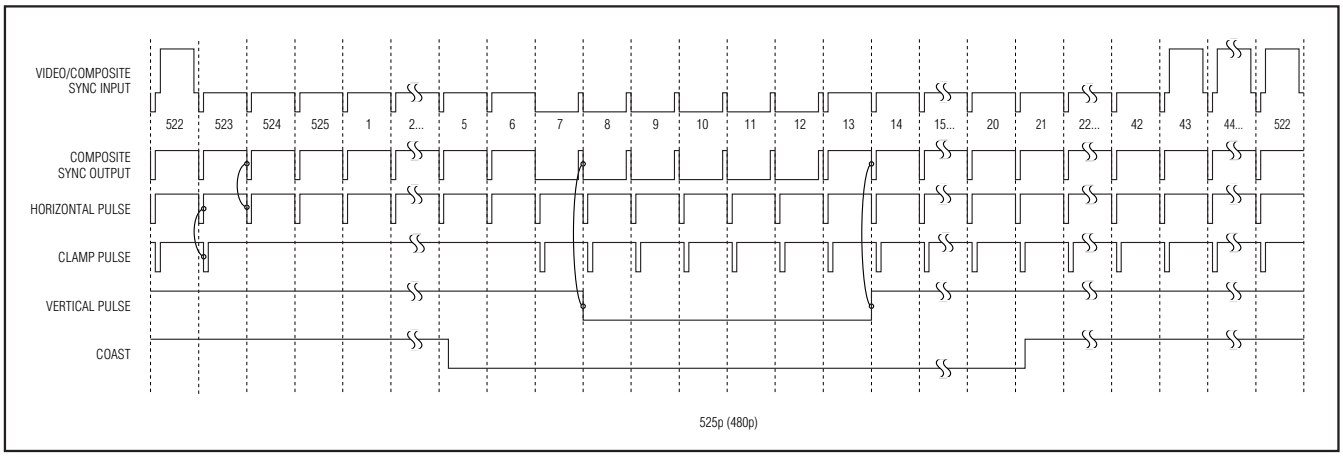


Figure1c. Extended Standard Progressive 525p (480p) Component Video

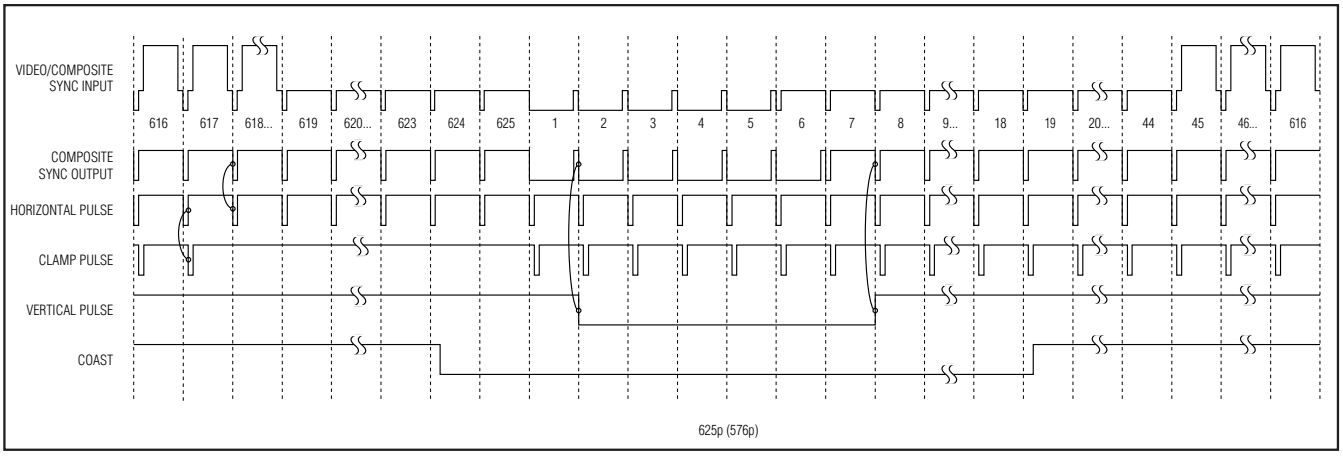


Figure1d. Extended Standard Progressive 625p (576p) Component Video

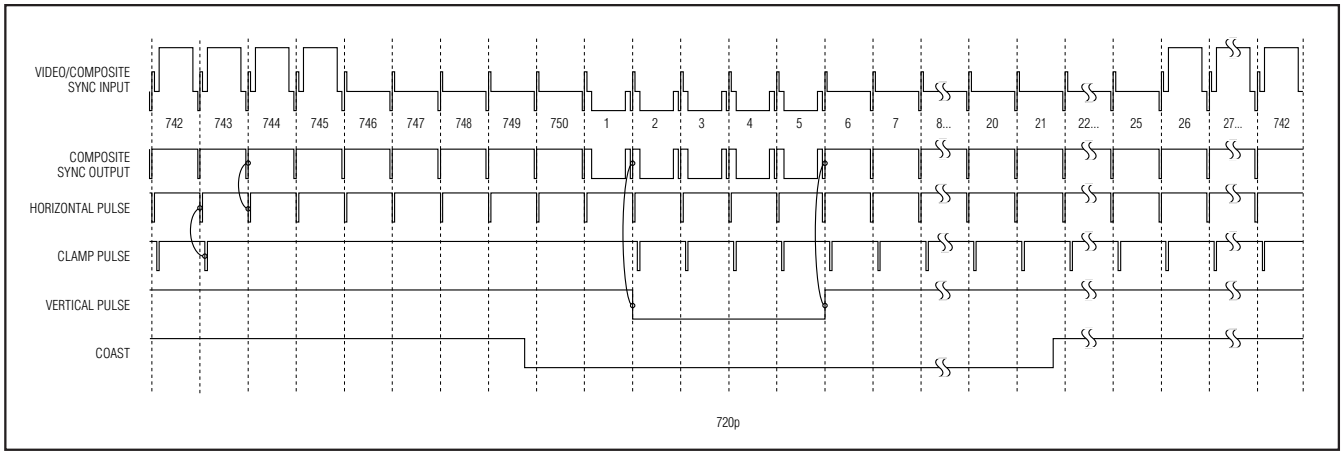


Figure1e. High-Definition Progressive 720p Composite Video

Component Analog TV Sync Separators

Timing Diagrams (continued)

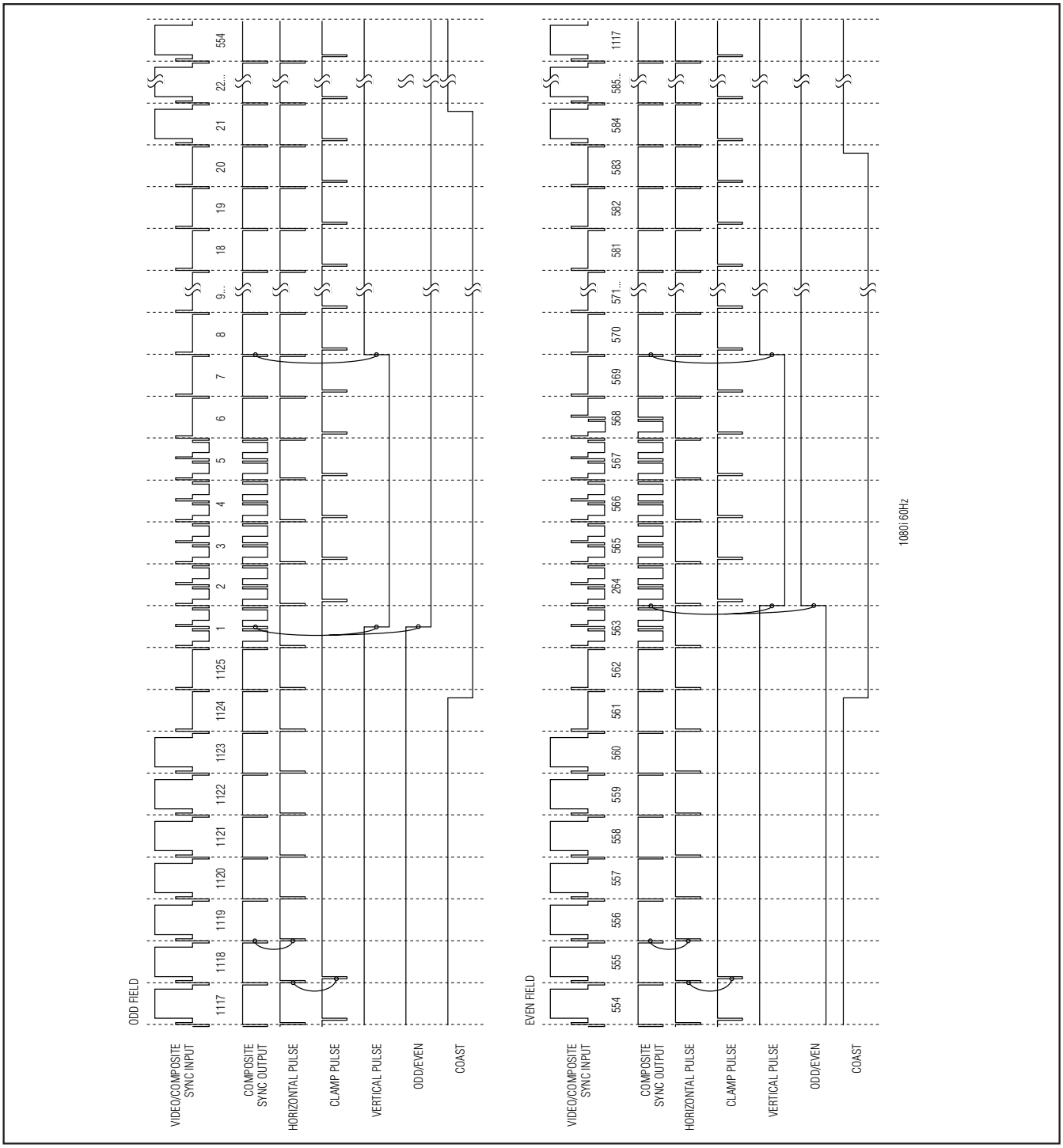


Figure1f. High-Definition Progressive 1080i Composite Video

Timing Diagrams (continued)

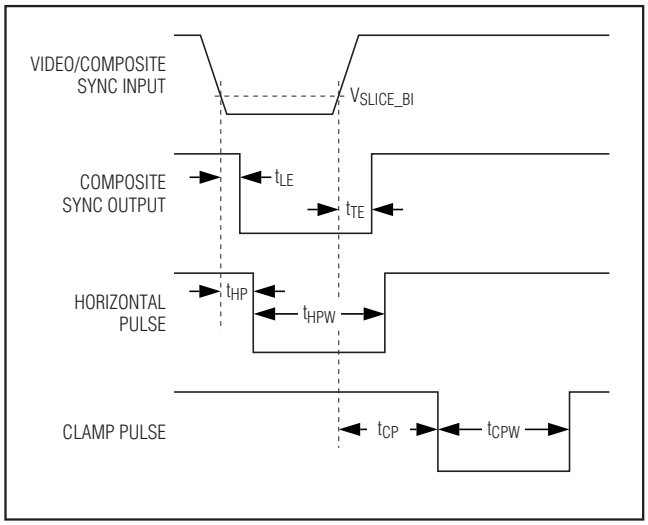


Figure2a. 525/625i 525/625p (480p/576p) Horizontal Timing

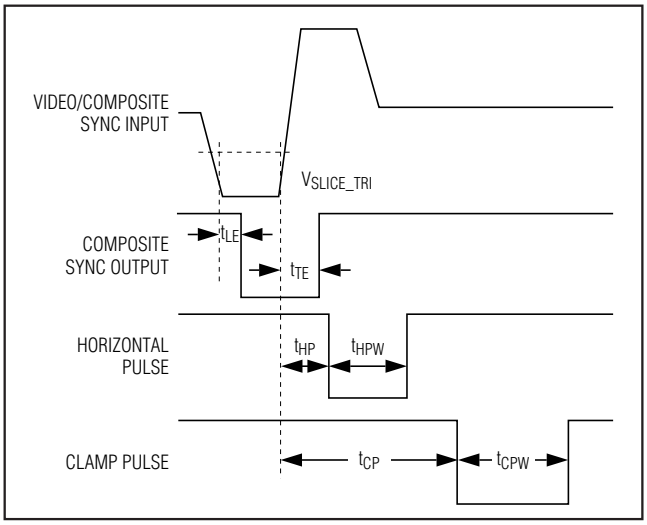
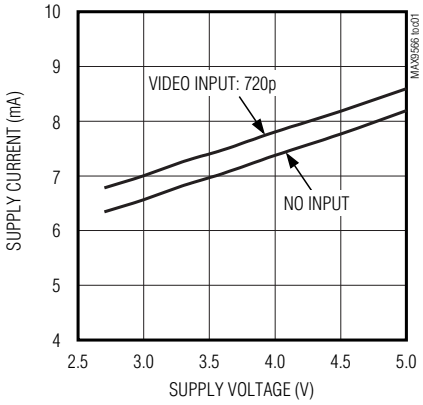


Figure2b. 720p/1080i Horizontal Timing

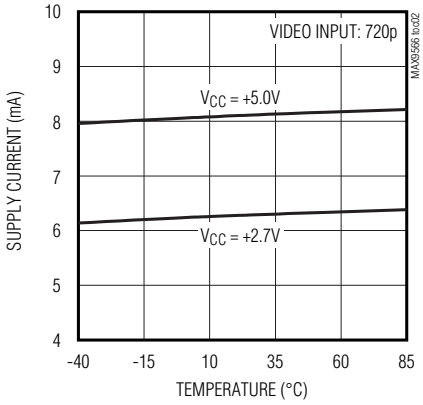
Typical Operating Characteristics

(V_{CC} = +5V, V_{GND} = 0V, T_A = +25°C, unless otherwise noted.)

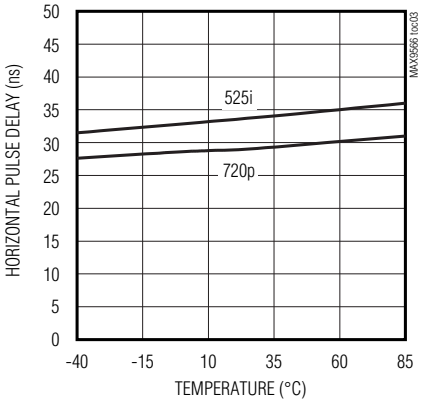
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



HORIZONTAL PULSE DELAY vs. TEMPERATURE

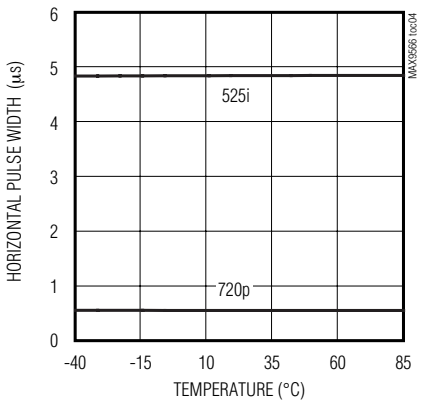


Component Analog TV Sync Separators

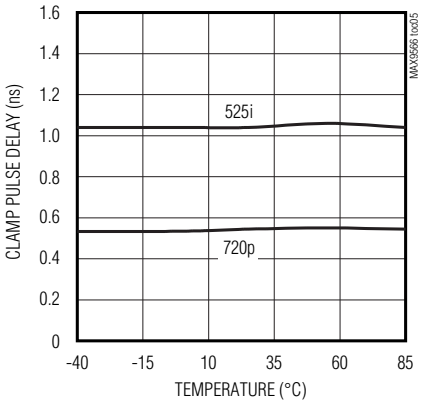
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{GND} = 0V, T_A = +25°C, unless otherwise noted.)

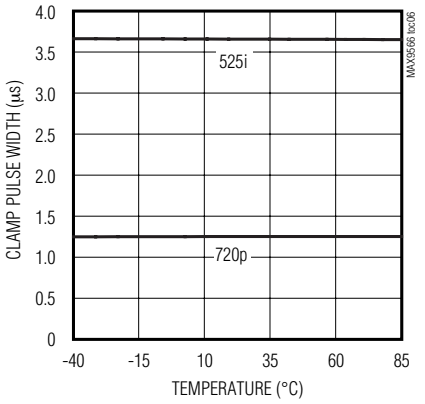
HORIZONTAL PULSE WIDTH vs. TEMPERATURE



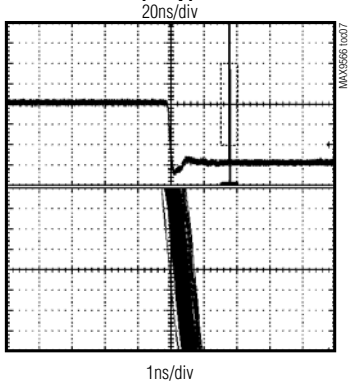
CLAMP PULSE DELAY vs. TEMPERATURE



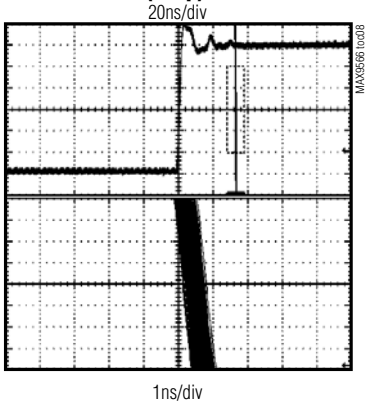
CLAMP PULSE WIDTH vs. TEMPERATURE



HORIZONTAL PULSE JITTER (576p)



HORIZONTAL PULSE JITTER (720p)



Pin Description

PIN				NAME	FUNCTION
MAX9566	MAX9567	MAX9568	MAX9569		
1	1	1	1	$\overline{CSYNCOUT}$	Composite Sync Output. Active low.
2	2	2	2	CVIDIN	Component Video Input
3	3	3	3	$\overline{VSYNCOUT}$	Vertical Timing Pulse Output. Active low.
4	4	5, 8	4	GND	Ground
5	5	12	—	$\overline{CLAMP}$	Clamp Pulse Output. Active low during the back porch portion of component video.
6	—	14	—	$\overline{ODD}$/EVEN	Odd and Even Line Field Output. Indicates odd or even field for interlaced video standards. $\overline{ODD}$/EVEN is logic-high for even fields and logic-low for odd fields.
7	7	15	7	$\overline{HSYNCOUT}$	Horizontal Timing Pulse Output. Active low.
8	8	16	8	V_{CC}	Positive Supply. Bypass V_{CC} to GND with a 0.1µF capacitor.
—	6	13	6	$\overline{LOS}$	Loss-of-Sync Output. Indicates the presence of a video input signal. Active low.
—	—	4	—	$\overline{COAST}$	Coast Output. Active low.
—	—	6	—	FR	Frame Rate Output. FRAME high indicates 60Hz and low indicates 50Hz. See Table 1.
—	—	10	5	SDTV	Standard Output 1. SDTV high indicates standard-definition television. SDTV low indicates extended definition or high-definition television. See Table 1.
—	—	11	—	HDTV	Standard Output 2. HDTV high indicates high-definition television. HDTV low indicates standard-definition or extended definition television. See Table 1.
—	—	7	—	HL	Standard Output 3. HL high indicates 625i, 625p (576p), and 1080i standards. HL low indicates 525i, 525p (480p), and 720p standards. See Table 1.
—	—	9	—	N.C.	No Connection. Not internally connected.

Table 1. Video Standard Output Decoding

TV STANDARD	CLASSIFICATION	OUTPUT PINS			
		FR	SDTV*	HDTV*	HL
525i	SDTV	High	High	Low	Low
625i	SDTV	Low	High	Low	High
525p/480p	EDTV	High	Low	Low	Low
625p/576p	EDTV	Low	Low	Low	High
720p	HDTV	High	Low	High	Low
1080i/60	HDTV	High	Low	High	High
1080i/50	HDTV	Low	Low	High	High

**For MAX9569, SDTV high indicates a standard-definition component video signal. HDTV high indicates a high-definition component video signal.*

Component Analog TV Sync Separators

Detailed Description

The MAX9566–MAX9569 family of sync separators extract sync timing information from SDTV, EDTV, and HDTV component video signals. The MAX9566–MAX9569 are stand-alone devices, and require no external components to set timing or bias voltage. The MAX9566–MAX9569 have high input impedance, eliminating the need for a low-impedance video source at the input.

The MAX9566–MAX9569 provide composite sync, vertical sync, and horizontal sync outputs. The MAX9568/MAX9569 provide automatic SDTV, EDTV, and HDTV detection logic outputs to indicate the type of TV standard being processed. The MAX9566/MAX9567/MAX9568 provide a back-porch clamp output signal.

The MAX9567/MAX9568/MAX9569 provide a loss-of-sync output to indicate a loss-of-video input signal. The MAX9566/MAX9568 provide an output to indicate odd and even fields. The MAX9568 provides a vertical interval coast output which allows control of a PLL oscillator when coasting through the vertical interval.

Component Video Input (CVIDIN)

CVIDIN provides a high input impedance to the analog video source. This eliminates the requirement for a low-impedance video source. Following the input buffer is the sync slicer block. This block establishes a DC level for the incoming video signal. The sync information is stripped by using a comparator with threshold or slice level that automatically adjusts to the incoming signal. When the incoming signal has bilevel syncs, the slice is made 95mV above the sync tip. When the incoming signal has trilevel syncs, the slice is made 145mV above the sync tip. The device's wide dynamic range, 0.2V to V_{CC} - 0.2V, allows the video signal from $0.5V_{P-P}$ to $2V_{P-P}$ to be processed and operate in the linear range. The mentioned threshold levels are independent of the signal amplitude.

CVIDIN is biased to 0.35 x V_{CC} through a 300kΩ resistor. Use a 0.1µF capacitor to AC-couple at the input if the input signal is not within the input-voltage range, as shown Figure 3.

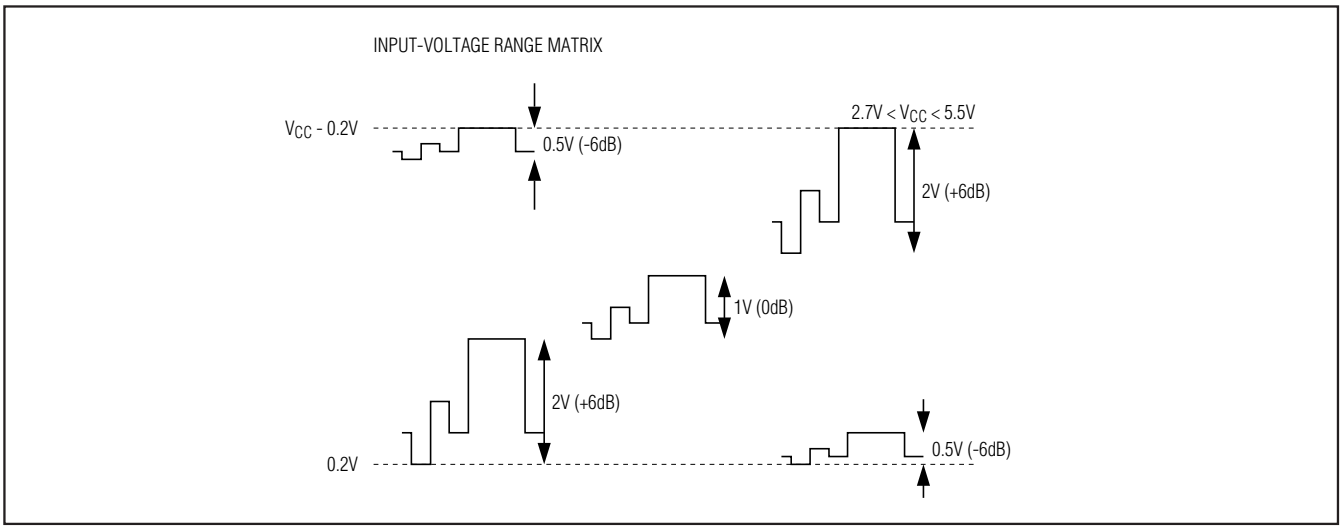


Figure 3. Input-Voltage Range Matrix

Composite Sync Output ($\overline{CSYNCOUT}$)

$\overline{CSYNCOUT}$ reproduces the component video input waveform with the active video removed. This output contains all the information below the component video black level. $\overline{CSYNCOUT}$ is pulled high whenever sync is not detected at the component video input. See Figures 2a and 2b for composite sync output timing diagrams.

Vertical Sync Output ($\overline{VSYNCOUT}$)

$\overline{VSYNCOUT}$ produces a pulse signal that defines the beginning of a new field in interlaced systems or frame in progressive systems. This output pulses low whenever the vertical sync pulse interval is detected. See Figure 4 for vertical sync output timing diagrams.

Horizontal Sync Output ($\overline{HSYNCOUT}$)

$\overline{HSYNCOUT}$ produces a pulse signal that defines the beginning of the horizontal line. This output pulses low whenever a horizontal sync pulse is detected. For interlace standards, the horizontal pulse output rate remains constant. See Figures 2a and 2b for horizontal sync output timing diagrams.

Standard- and High-Definition TV Detection (SDTV, HDTV, HL)

SDTV, HDTV, and HL produce logic outputs that indicate the standard of the component video signal at the input. SDTV output high indicates standard-definition television while SDTV output low indicates extended definition or high-definition television.

HDTV output high indicates high-definition television while HDTV output low indicates standard-definition or extended definition television.

HL output high indicates 625i, 625p (576p), and 1080i standards while HL output low indicates 525i, 525p (480p), and 720p standards. See Table 1.

Loss-of-Sync Output ($\overline{LOS}$)

$\overline{LOS}$ produces logic output that indicates the presence of a video input signal. $\overline{LOS}$ output high indicates that there is a sync or video signal at the input while $\overline{LOS}$ low indicates the presence of a component video signal at CVIDIN.

Clamp Pulse Output ($\overline{CLAMP}$)

$\overline{CLAMP}$ produces a pulse signal that is generally used to drive a black-level clamp circuit which restores the DC component to a video signal. This output pulses low during black-level (back porch) of each video line. See Figures 2a and 2b for clamp pulse output timing diagrams.

Coast

The MAX9568 provides a vertical interval coast output which allows the PLL oscillator to coast through the vertical interval. This output pulses low during vertical blanking interval.

Odd and Even Field Detection ($\overline{ODD}$/EVEN)

$\overline{ODD}$/EVEN produces a square wave that identifies the present field of an interlaced video source. $\overline{ODD}$/EVEN output low indicates odd field while $\overline{ODD}$/EVEN output high indicates even field. This square wave changes coincidentally with the beginning of the vertical pulse.

Applications Information

Chroma Filter

If the input signal is standard-definition composite video, a simple lowpass filter is recommended in front of the input to attenuate the chroma signal, or any high-frequency noise below the black level. As shown in Figure 5, when the input is standard-definition video, SDTV (MAX9568/MAX9569 only) is logic-high and Q1 is turned on. When Q1 is on, R1 and C2 form a 600kHz lowpass filter to attenuate high-frequency noise and improve the performance of the MAX9568/MAX9569. When the input is high-definition video or extended definition video, SDTV is logic-low and Q1 is turned off, disabling the RC input filter.

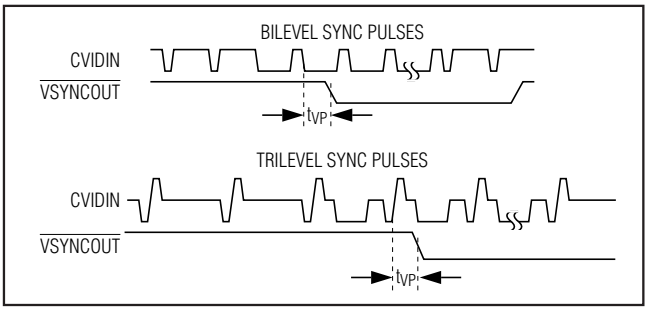


Figure 4. Vertical Sync Output Timing Diagrams

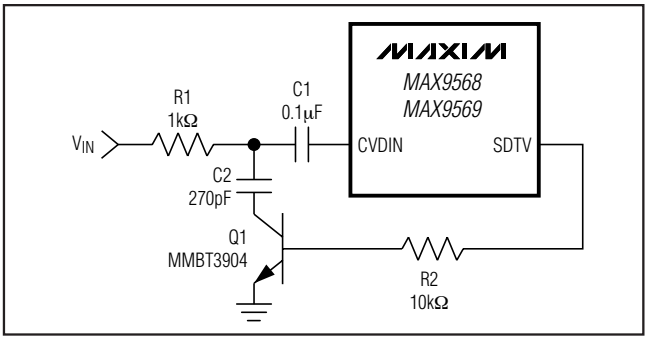
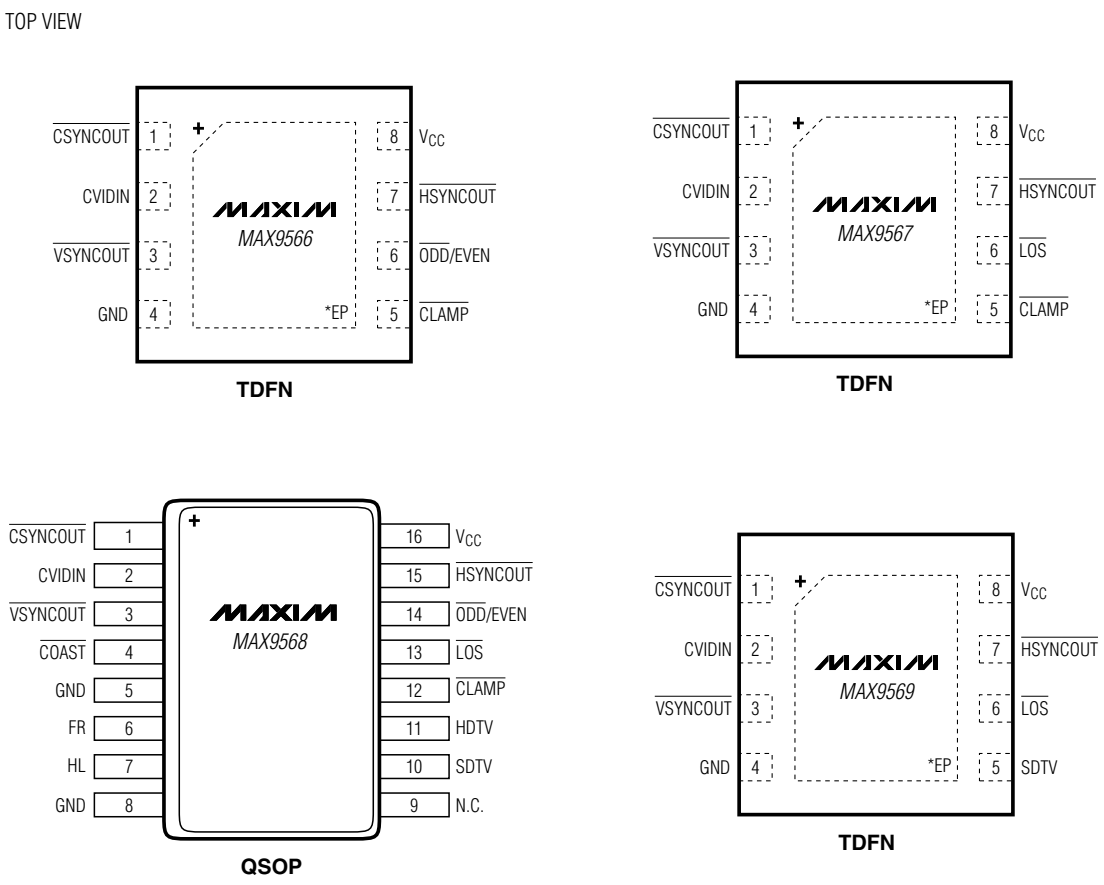


Figure 5. Chroma Filter

Component Analog TV Sync Separators

Pin Configurations



Ordering Information (continued)

PART	PIN-PACKAGE	TOP MARK
MAX9568EEE+T	16 QSOP	—
MAX9569ETA+T*	8 TDFN-EP**	ASZ

Note: *All devices are specified over the -40°C to +85°C operating temperature range.*

+Denotes a lead-free package.
T = Tape and reel.
**Future product—contact factory for availability.*
***EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
8 TDFN	T833-2	**21-0137**
16 QSOP	E16-1	**21-0055**